REMARKS

Applicant thanks the Examiner for the thorough consideration given the present application. Claims 1-4, 9-13, 15, 16 and 19-32 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

REJECTION UNDER 35 U.S.C § 102

Claims 1-4, 9-13, 15, 16 and 19-26 stand rejected under 35 U.S.C § 102 as being anticipated by Feldman (U.S. Patent 6,097,857). This rejection is respectfully traversed.

The Examiner states that Feldman shows an integrated module having a transparent substrate (17') which has a circuit layer formed on one surface for electrical interconnection and a plurality of electric paths (20'), at least two chips (13', 15') which are mounted on the transparent substrate by way of flip-chip bonding and a circuit substrate (45) having a circuit layer (40') and at least one gap between the chips and the circuit substrate. Applicants disagree with the Examiner's understanding of the Feldman reference and submit that these claims are not anticipated by this reference.

The embodiment shown in Figures 5 and 6 of Feldman include a heat sink (11') attached to a mounting substrate (45). Integrated circuit chips (13', 15') are mounted within the substrate so that their top surfaces are flush therewith. Holographic translator chips (46) are attached to the interconnection lines (40') on the surface of the substrate and also directly to chips (13', 15').

The Examiner has stated that transparent substrate (17') which is part of the interconnect chip (46) is an equivalent of the claim transparent substrate which forms the base for the entire claimed invention. The Examiner continues to point out that this transparent substrate has a circuit layer formed on the surface and a plurality of electrical pads (20'). Applicants agree that the chip (46) has this transparent substrate and these pads. However, this is part of a chip which

is mounted on the substrate (45) and not the other way around. Thus, when the Examiner states that this substrate has two chips (13', 15') which are mounted on the transparent substrate by

way of flip-chip bonding, this appears to be a reversal of the actual situation. As is clearly seen in Figure 5, chips (13', 15') are embedded in the surface of the substrate (45') and are not mounted on translator chip (46).

Further, it is noted that the last line of claim 1 describes the gap located between the chips and the circuit substrate. The chips are elements (13', 15') as indicated by the Examiner. Applicants submit that there is no gap. Instead, the two are joined directly together using flip-chip technology. The gap is designed to allow heat to escape from the chip. However, the direct bonding of the chips to the substrate through the contact pads (20', 22') and solder bump (24') will not allow such a gap for heat removal. Further, there is also no gap between the chips (13', 15') and the mounting substrate (45). Further, it is noted that an individual substrate (17') is associated with the single chip and not two chips as discussed in claim 1. Although there are electrical interconnections to more than one chip, only one chip can be "mounted on" the individual substrate even in the broadest sense of the word. For these reasons, Applicants submit that claim 1 is not anticipated by Feldman.

Claim 13 is a second independent claim which is also allowable over this reference. Clam 13 also describes that the two chips are connected to second bumps for electrical interconnection. At best, the Feldman reference can only associate one chip with the transparent substrate. Further, claim 13 describes the height of the first bumps as being larger than the height of the chips. This is clearly not seen in the reference.

Likewise, claim 21 is a third independent claim which also describes the two chips being mounted on the transparent substrate, which is not seen in the reference. Further, claim 21 describes the gap between the chips and the substrate in the same fashion as claim 1. Claim 21

further describes the hollow portion with chips being positioned in the hollow portion. This is clearly not seen in the reference in any manner.

Claims 2-4, 9-12, 15, 16, 19, 20 and 22-32 depend from these allowable independent claims and as such are also considered to be allowable. In addition, each of these claims recite other features which make them additionally allowable. Thus, claims 11, 12, 19 and 20 describe active and passive components formed under the transparent substrate which is not seen in the reference. Claim 25 describes a heat dissipation element formed on the back side of the chips which is not seen in the reference.

New claims 27, 29 and 31 describe that the chips are located on the same side of the transparent substrate as either the circuit substrate or the first bumps. Claims 28, 30 and 32 describe the pitch of the circuit being either below 100 micrometer or between 6 and 40 micrometer. These claims are considered to be additionally allowable as well.

Furthermore, as discussed in the specification, the transparent substrate (11) of the present application is a glass substrate so that its thermal expansion coefficient is similar to that of the semiconductor chip. Thus, the thermal variation influences the transparent substrate and the chips to a lesser extent. The result is that reliability is greatly improved due to the difference between the thermal expansion coefficients. In addition, transparent substrate (11) provides an excellent insulation property and reduces the decay of high frequency signals caused by parasitic capacitance and parasitic leakage resistance even if the sizes and pitches of the circuit for electrical interconnection in the chips are of the same order of magnitude. Thus, the integrated circuit of the present invention has superior high frequency properties. Thus, the transparent substrate (11) being made of glass is suitable to integrate multiple dies or chips to form a module as a circuit system.

Since the sizes and pitches can be reduced to the order of magnitude of the sizes and pitches of the chips, the overall size of the module can be reduced. The Feldman reference does not teach the pitches of the interconnection lines being below 100 micrometer. Accordingly, Applicant submits that the claims are additionally allowable.

CONCLUSION

In view of the above remarks, it is believed that the claims clearly distinguish over the patent relied on by the Examiner. In view of this, reconsideration of the rejection and allowance of all the claims are respectfully requested.

Applicants' undersigned representative remains ready to assist the Examiner in any way to facilitate and expedite the prosecution of this matter. If any point remains an issue in which the Examiner feels would be best resolved through a personal or telephone interview, please contact Robert F. Gnuse, Reg. No. 27,295 at the telephone number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

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Respectfully submitted,

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